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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,159	09/26/2001	Shakuntala Anjanaiah	TI-33534	9580

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EXAMINER	
GREY, CHRISTOPHER P	
ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/964,159	Applicant(s) ANJANAIAH ET AL.	
	Examiner Christopher P Grey	Art Unit 2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

(a) The examiner requests that the related applications, application numbers be provided, as they are missing on page 1 lines 11-25.

(b) Grammatical error on page 3 line 9, "increases the both the".

(c) Grammatical error on page 14 line 10, "The process than returned".

(d) Incomplete sentence on page 16 line 29, "access unit is a part"

Appropriate correction is required.

Claim Objections

2. Claims 12 and 17 are objected to because of the following informalities:

" The method as recited in claim 11 wherein 1".

The statement, "wherein 1" should be excluded from both claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5-8 and 10 are rejected under 35 U.S.C. 102(b)as being anticipated by Oskouy et al. (US 5625625).

Claim 1 Oskouy ('Oskouy' hereinafter) discloses an interface unit between a communication bus (element 138 in fig 8) and a media (element 140).

Oskouy discloses a receive channel connecting the system bus to a system bus interface (fig 8 elements 138 and 120). The data received via the receive interface is forwarded to a system and ATM Layer Core (data processing unit) as disclosed in fig 8 element 122.

Oskouy discloses the system and ATM layer core transmitting data cells to the media via a transmit channel connecting the media interface and the media (fig 8 elements 122, 132 and 140 and Col 10 lines 35-49).

Oskouy discloses a media interface (ATM interface mode), where the media interface operates according to an ATM protocol (Col 10 lines 24-28 and fig 8 element 132). Oskouy also discloses an I/O interface (element 124 in fig 8 and Col 11 lines 9-25).

Claim 2 Oskouy discloses the media interface conforming to a UTOPIA standard (Col 10 lines 50-64) and an I/O interface (element 124 in fig 8 and Col 11 lines 9-25).

Claim 3 Oskouy discloses the entire interface unit (element 112 in fig 8) functioning as a direct memory access controller (Col 10 lines 35-49) and possibly a DMA controller being employed (Col 5 lines 59- Col 6 lines 8).

Claim 5, 10 Oskouy discloses an I/O interface (element 124 in fig 8 and Col 11 lines 9-25).

Oskouy discloses a media interface (output interface) as disclosed in Col 10 lines 24-28 and fig 8 element 132.

Oskouy discloses a receive FIFO buffer (element 130 in fig 8) and a receive mode, where receiving data into the buffer is scheduled (Col 9 lines 25-33). Oskouy also discloses a direct memory access controller assisting in the transfer of data (Col 8 lines 49-60).

Oskouy discloses a transmit FIFO buffer (element 128 in fig 8) and a transmit mode implementing a direct memory access controller (Col 5 lines 59- Col 6 lines 8). Oskouy discloses an unload engine scheduling the operation of a load engine, where the unload engine transmits data from the buffer memory (Col 7 lines 58-Col 8 line 15).

Claim 6 Oskouy discloses a transmit mode, where a signal is initiated indicating that a new packet is available. Oskouy also discloses a response to this signal, where scheduling occurs. Oskouy also indicates whether a queue is full or empty (Col 6 lines 21-44). Oskouy also discloses a receive mode (Col 8 line 44-Col 9 line 67).

Claim 7 Oskouy discloses a first set of signals entering an interface (element 112 in fig 8) being exchanged from Media (element 140), where the media interface

(element 132) operates according to an ATM protocol (Col 10 lines 24-28 and fig 8 element 132).

Oskouy discloses a second set of signals entering an interface (element 112) from a system bus (element 138 in fig 8), where the data is exchanged via an I/O interface (element 124 in fig 8).

Claim 8 Oskouy discloses the media interface conforming to a UTOPIA standard (Col 10 lines 50-64) and an I/O interface (element 124 in fig 8 and Col 11 lines 9-25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 and 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oskouy et al. (US 5625625) in view of Jensen et al. (US 6732206)

Claim 4 Oskouy discloses an I/O interface and ATM interface as disclosed in the rejection of claim 1. Oskouy does not disclose a control register determining when the interface unit is in the ATM mode of operations and when the interface is in the I/O mode of operation.

Jensen et al. ('Jensen' hereinafter) discloses a slave unit comprising an address translator, which contains an ATM content memory and a SRAM look up table (control

register). Jensen discloses translating an incoming address (I/O interface mode) to a destination address (ATM interface mode) as disclosed in Col 2 lines 8-45.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the interface (element 112 in fig 8) as disclosed by Oskouy, to contain an address translator, where translating an address would indicate a change in mode at the interface. The motivation for this modification is to alleviate an address shortage (Col 2 lines 8-23).

Claim 11 Oskouy discloses first and second sets of signals as disclosed in the rejection of claim 7. Oskouy does not disclose a control register for storing these signals. Jensen discloses a slave unit comprising an address translator, which contains an ATM content memory and a SRAM look up table (control register) as disclosed in Col 2 lines 836-45.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the interface (element 112 in fig 8) as disclosed by Oskouy, to contain an address translator, where in order to translate an address, the incoming address must be temporarily stored. The motivation for this modification to expand addressing (Col 1 lines 33-42).

Claim 12, 17 Oskouy discloses a transmit mode, where a signal is initiated indicating that a new packet is available. Oskouy also discloses a response to this signal, where scheduling occurs. Oskouy also indicates whether a queue is full or empty (Col 6 lines 21-44). Oskouy also discloses a receive mode (Col 8 line 44-Col 9 line 67).

Claim 13 Oskouy discloses a system bus interface (fig 8 element 120) for coupling to a system bus (element 138 in fig 8).

Oskouy discloses a processor (element 112).

Oskouy discloses a first set of signals entering an interface (element 112 in fig 8) being exchanged from Media (element 140), where the media interface (element 132) operates according to an ATM protocol (Col 10 lines 24-28 and fig 8 element 132).

Oskouy discloses an I/O interface (element 124 in fig 8) where a second set of signals entering an interface (element 112) from a system bus (element 138 in fig 8), where the data is exchanged via an I/O interface (element 124 in fig 8).
Oskouy does not disclose a control register for storing signals. Jensen discloses a slave unit comprising an address translator, which contains an ATM content memory and a SRAM look up table (control register) as disclosed in Col 2 lines 836-45.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the interface (element 112 in fig 8) as disclosed by Oskouy, to contain an address translator, where in order to translate an address, the incoming address must be temporarily stored. The motivation for this modification to expand addressing (Col 1 lines 33-42).

Claim 14 Oskouy discloses the media interface conforming to a UTOPIA standard (Col 10 lines 50-64) and an I/O interface (element 124 in fig 8 and Col 11 lines 9-25).

Claim 15 Oskouy discloses an I/O interface (element 124 in fig 8 and Col 11 lines 9-25).

Oskouy discloses a media interface (output interface) as disclosed in Col 10 lines 24-28 and fig 8 element 132.

Oskouy discloses a receive FIFO buffer (element 130 in fig 8) and a receive mode, where receiving data into the buffer is scheduled (Col 9 lines 25-33). Oskouy also discloses a direct memory access controller assisting in the transfer of data (Col 8 lines 49-60).

Oskouy discloses a transmit FIFO buffer (element 128 in fig 8) and a transmit mode implementing a direct memory access controller (Col 5 lines 59- Col 6 lines 8). Oskouy discloses an unload engine scheduling the operation of a load engine, where the unload engine transmits data from the buffer memory (Col 7 lines 58-Col 8 line 15).

Claim 16 Oskouy discloses the entire interface unit (element 112 in fig 8) functioning as a direct memory access controller (Col 10 lines 35-49) and possibly a DMA controller being employed (Col 5 lines 59- Col 6 lines 8).

5. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oskouy et al. (US 5625625)

Claim 9 Oskouy does not disclose the processor being a digital signal processor.

The background of the invention discloses a data processing system using a digital signal processor (page 2 lines 1-24).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the interface unit as disclosed by Oskouy to function as a digital

signal processor. The motivation for this modification is to enable the interface unit to respond to a wide variety of computational intensive requirements.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(a) Wing So (US 6141744) discloses an interface device between a master and slave device containing a FIFO buffer, a register and digital signal processors.

(b) Watkins (US 5983332) discloses an apparatus and method for translating an address, containing FIFO buffers, memory, address translation unit and processors.

(c) Kessler et al. (US 6029212) discloses a method of accessing a memory location within a system having a processor and a plurality of memory locations separate from the processor.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571)272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher Grey
Examiner
Art Unit 2667

C. Grey
5/9/05

A. Qureshi 5/11/05
AFSAR QURESHI
PRIMARY EXAMINER